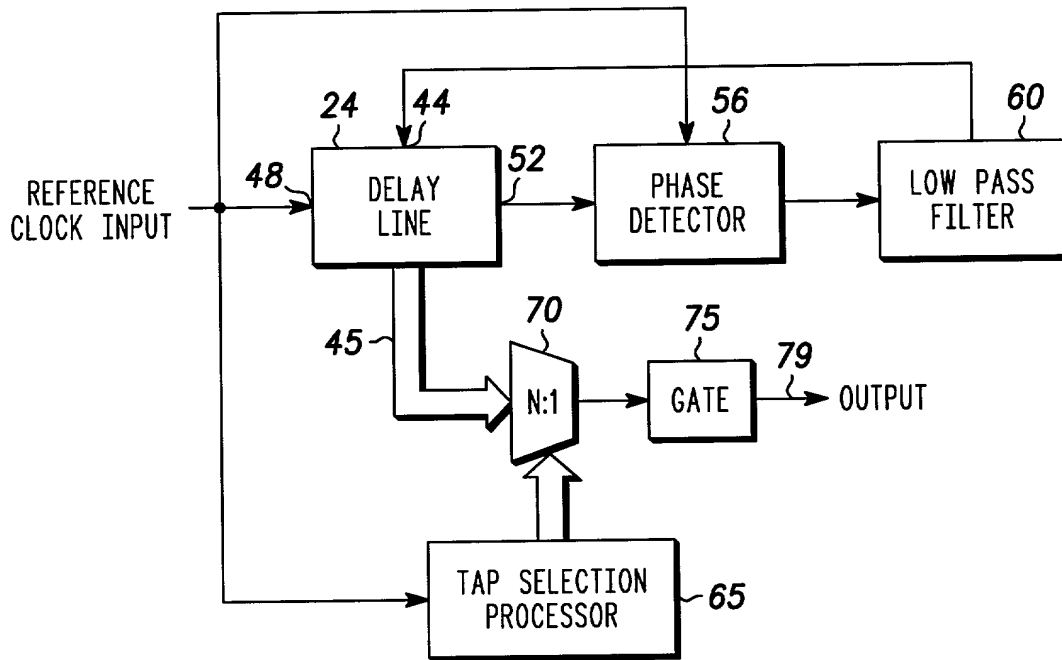


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FIG.1

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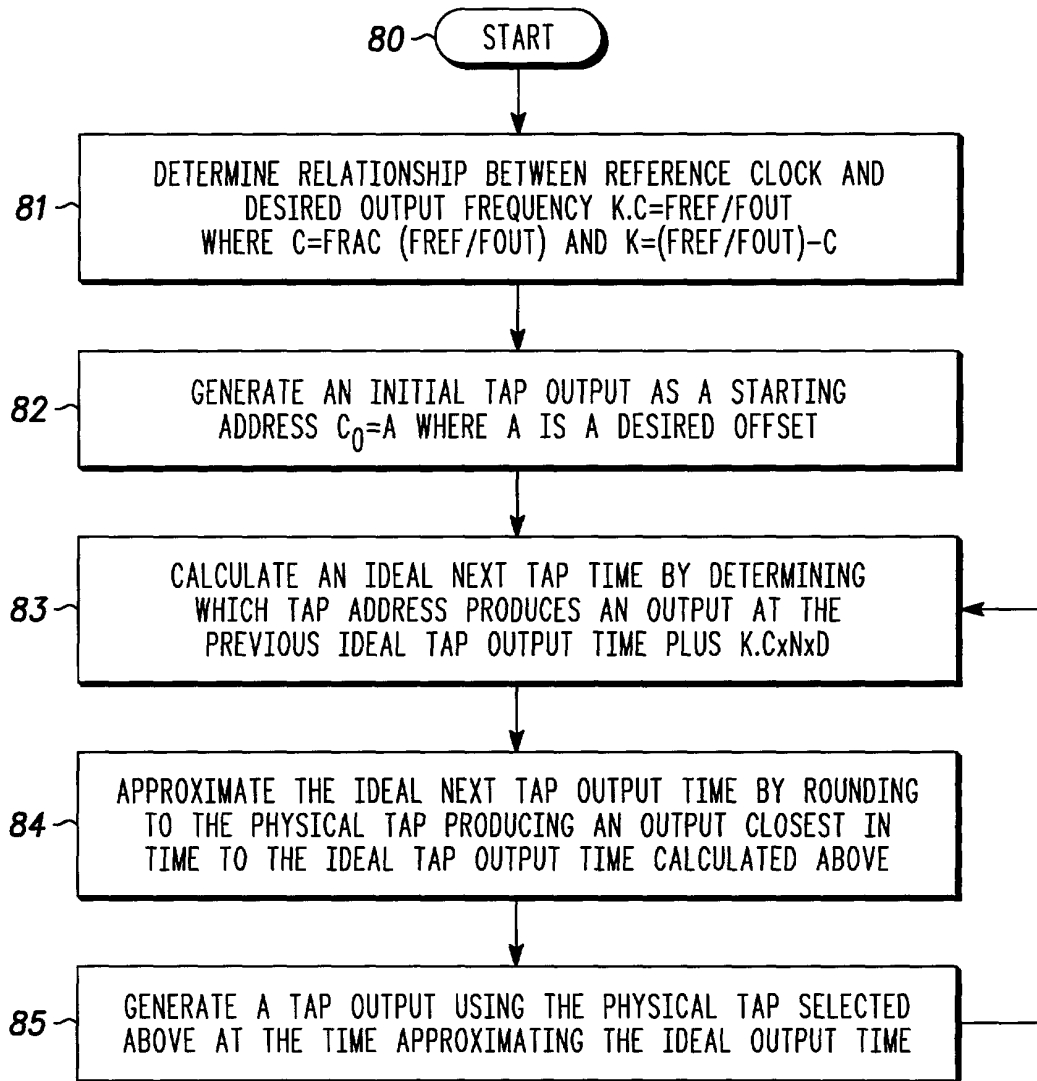


FIG. 2

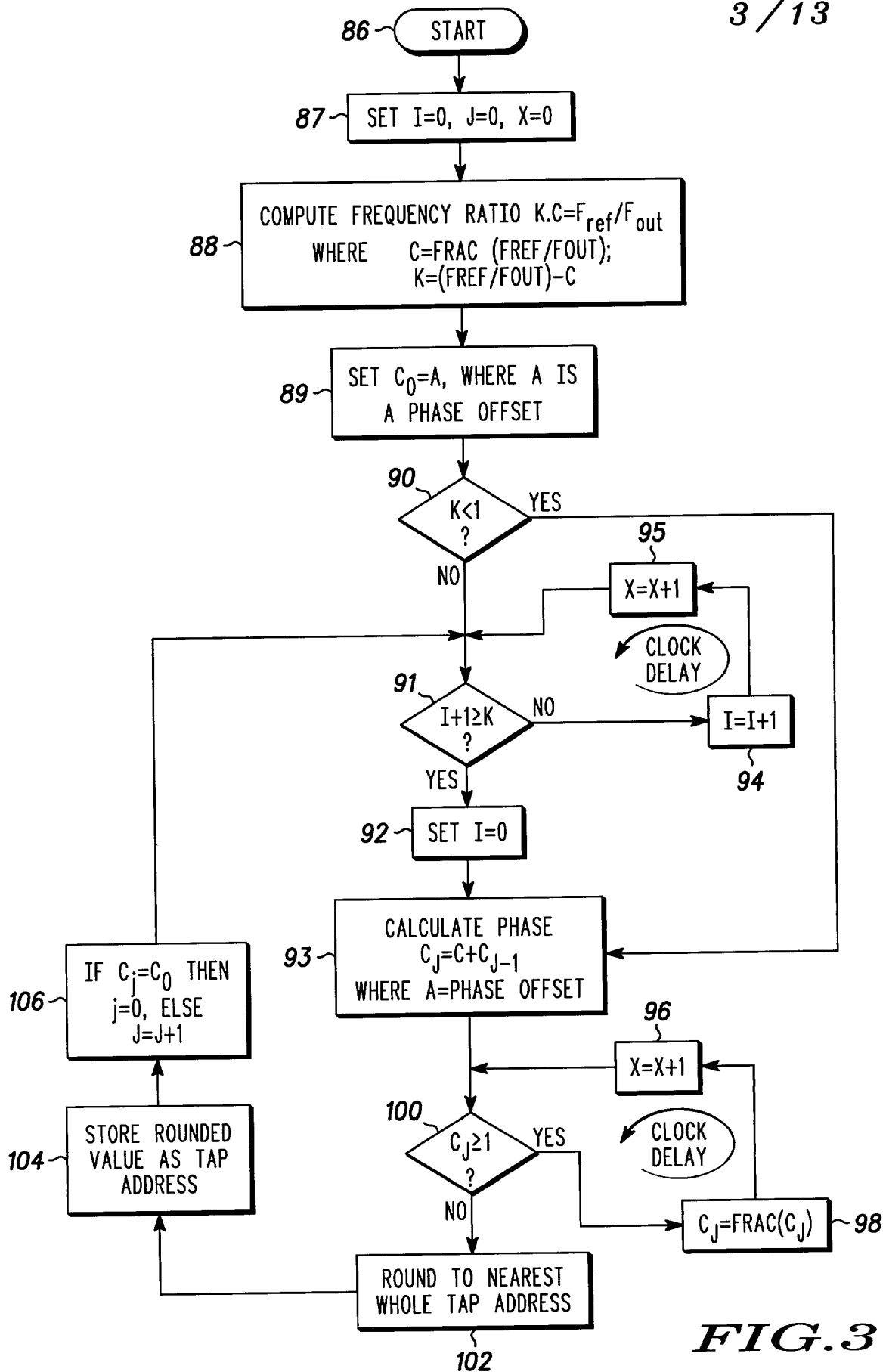


FIG.3

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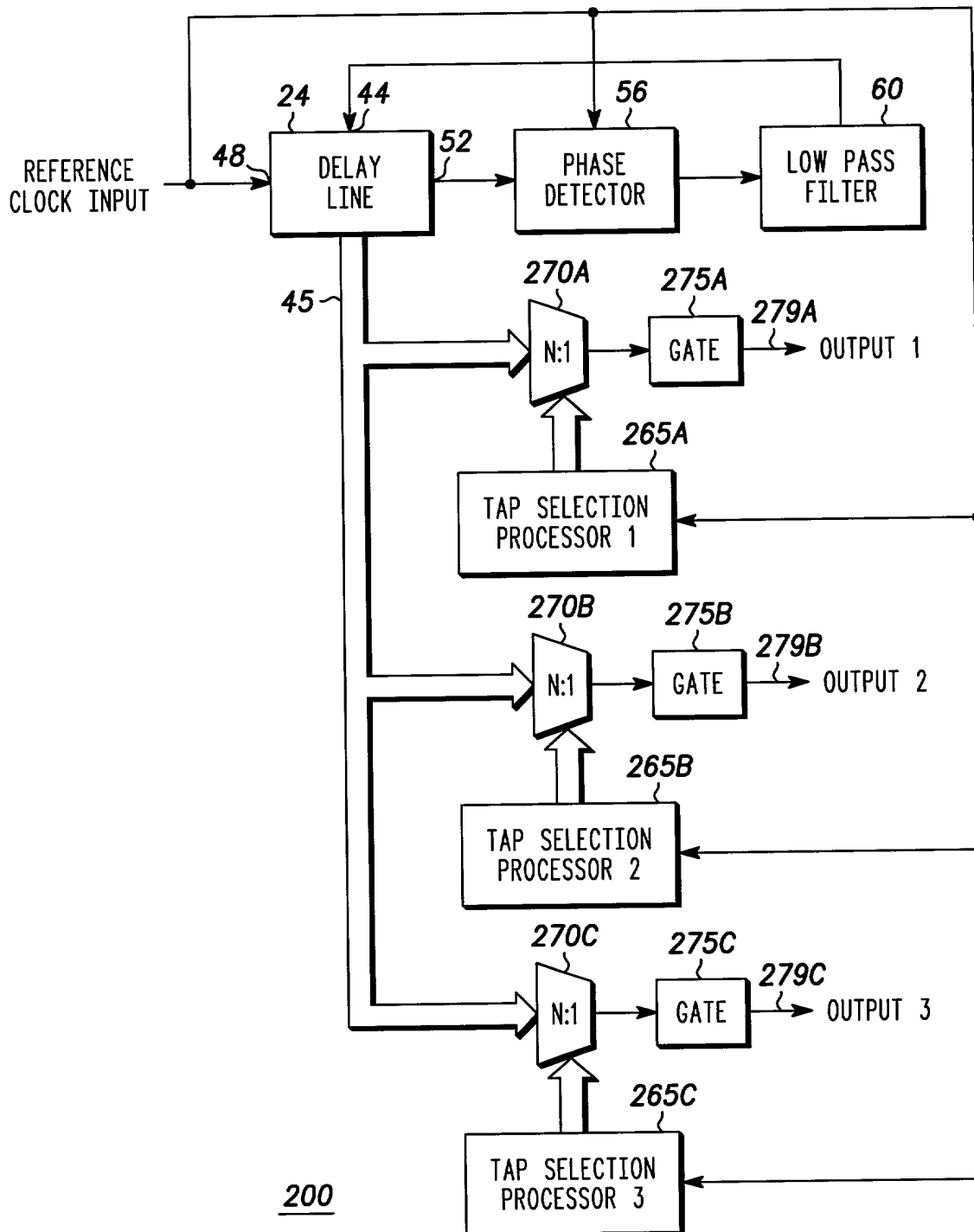


FIG. 4

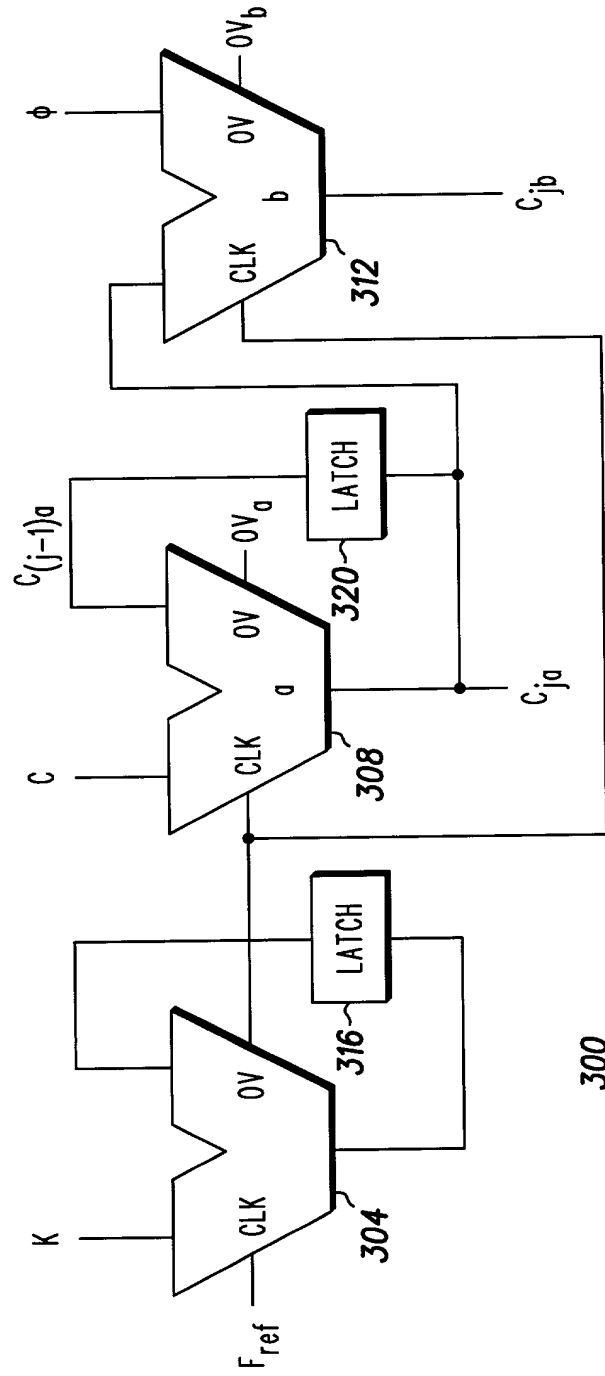


FIG. 5

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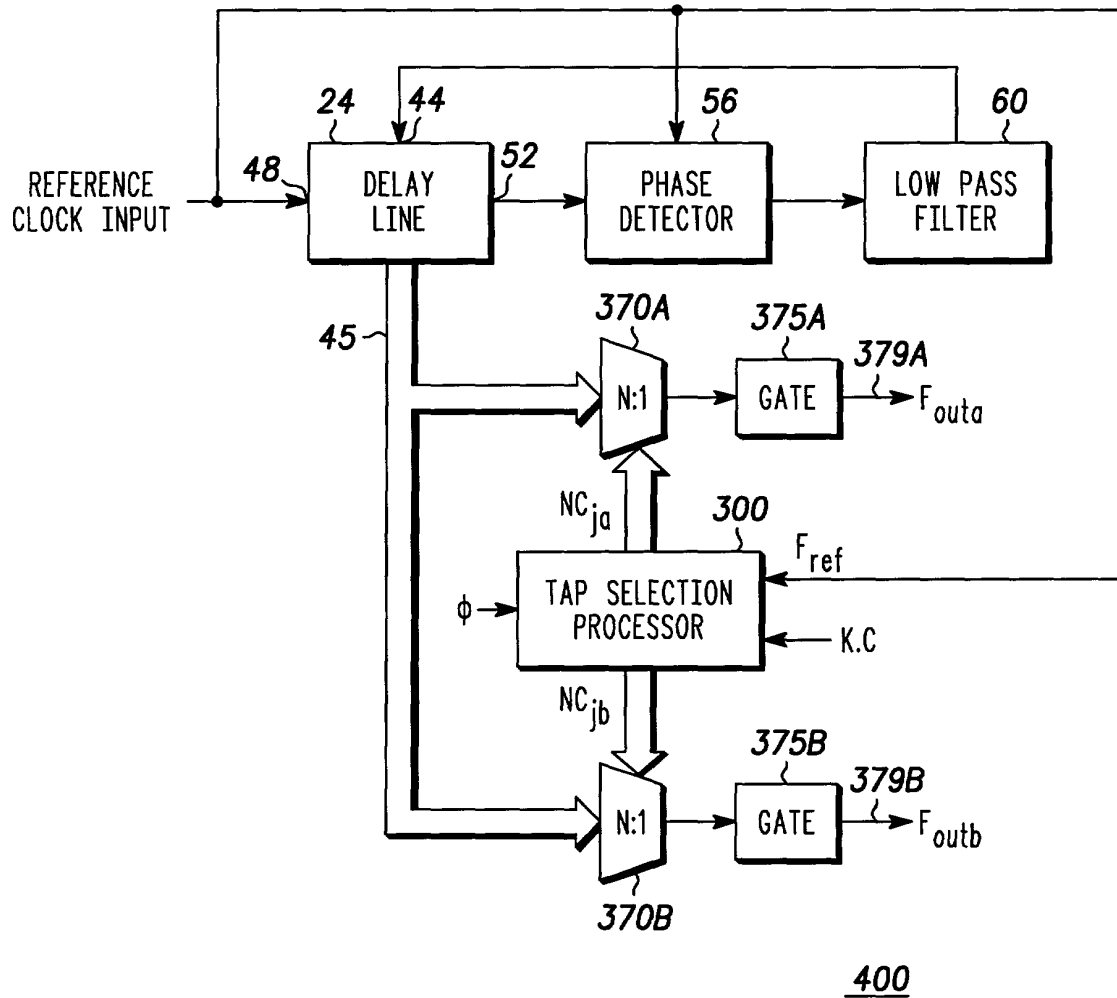


FIG. 6

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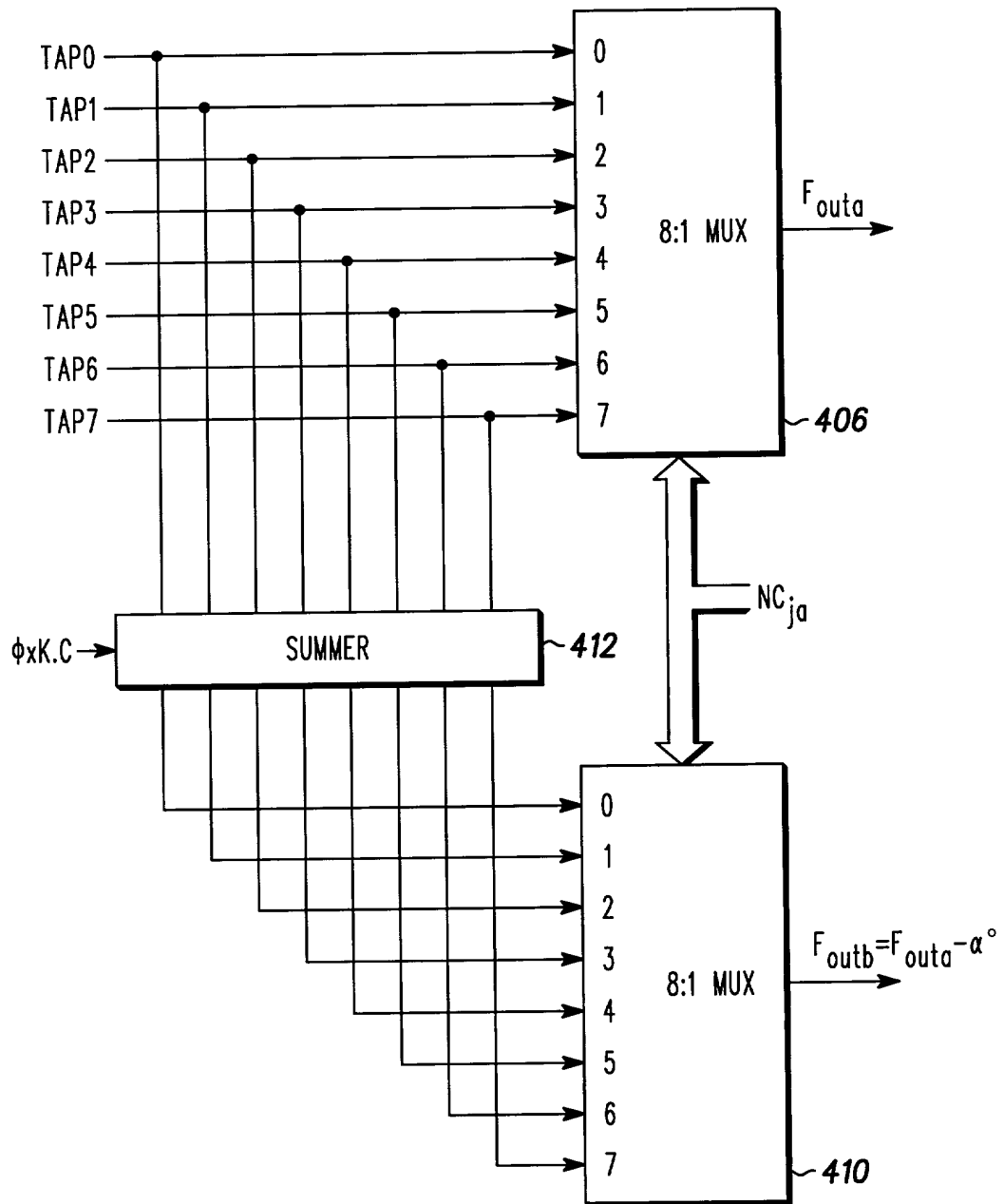


FIG. 7

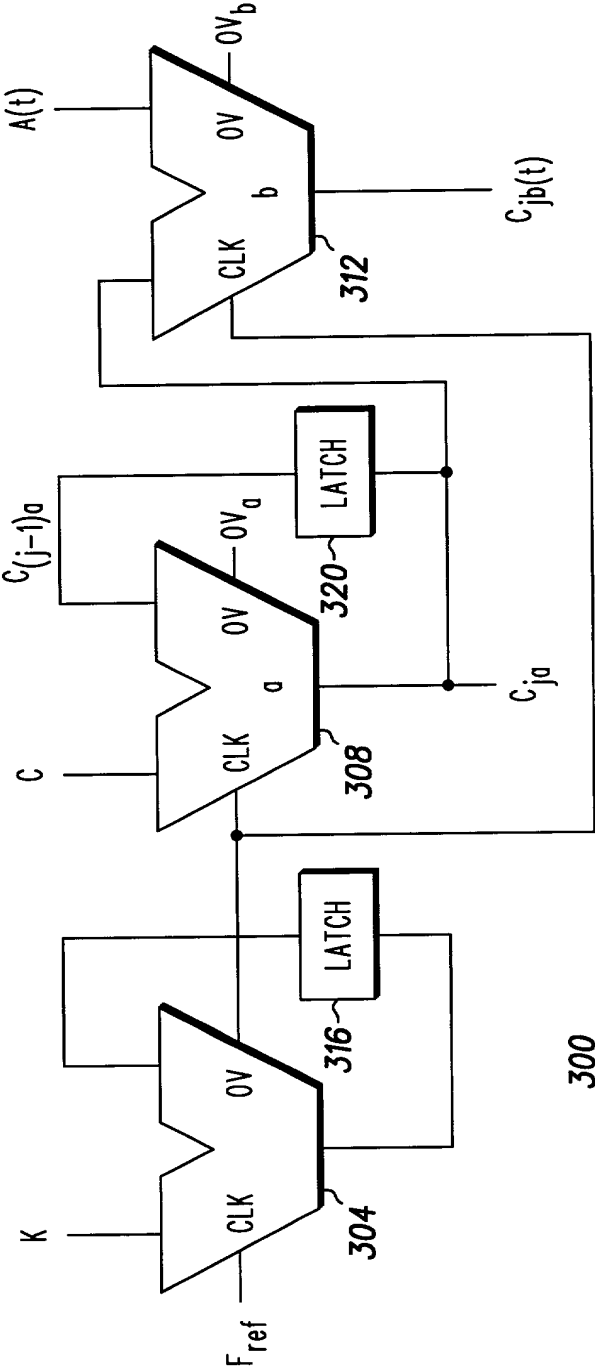


FIG. 8

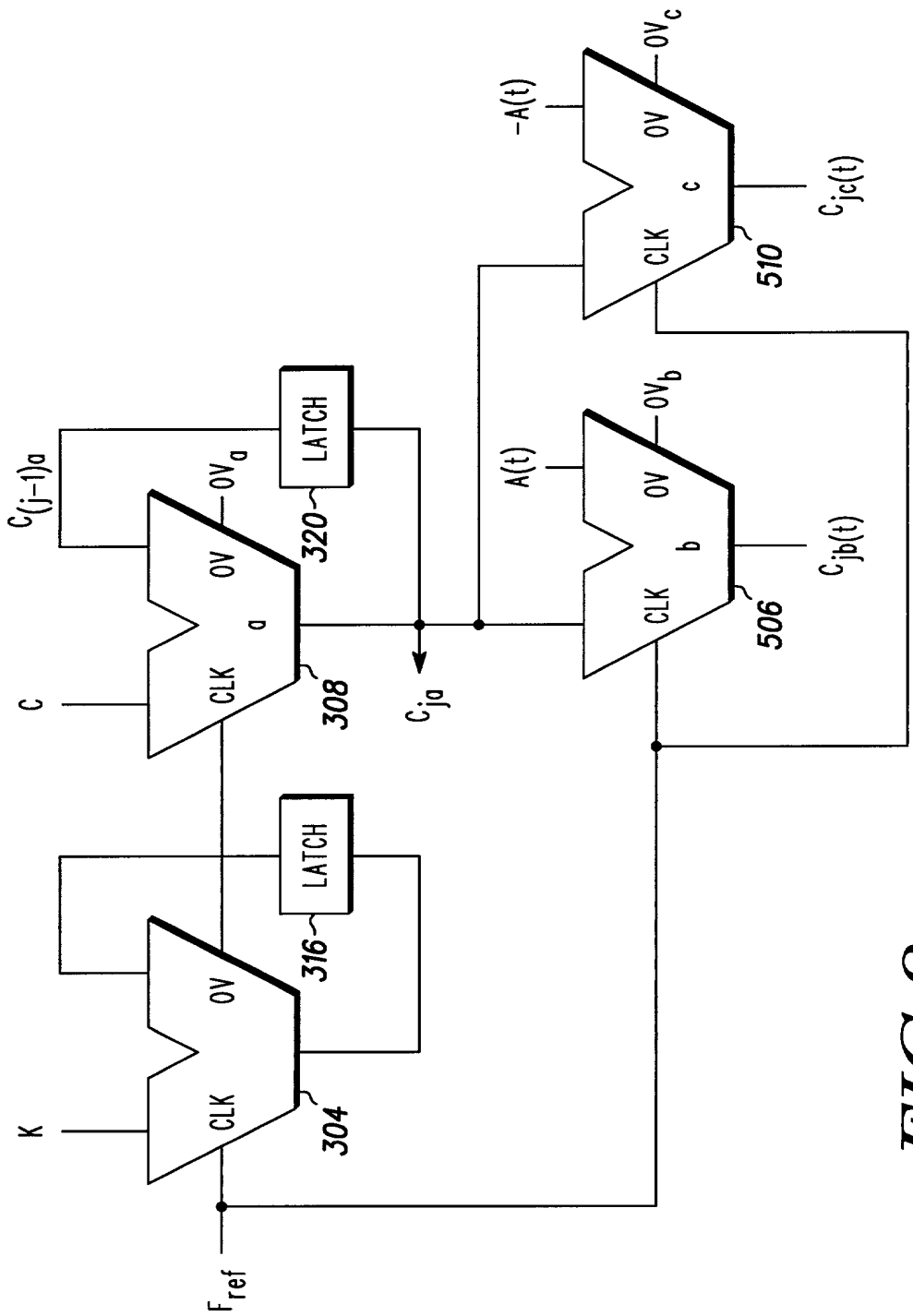


FIG. 9

FIG. 9 is a block diagram of a circuit for processing a signal. The circuit includes a series of comparators and latches. The comparators are labeled 304, 316, 308, 320, 506, and 510. The latches are labeled LATCH. The circuit is controlled by a common clock signal CLK and a reference signal Fref. The comparators receive inputs K, C, C(j-1)a, A(t), and -A(t). The comparators 308 and 506 output signals Cja and Cjb(t) respectively. The comparators 510 and 506 output signals Cjc(t) and Cjb(t) respectively.

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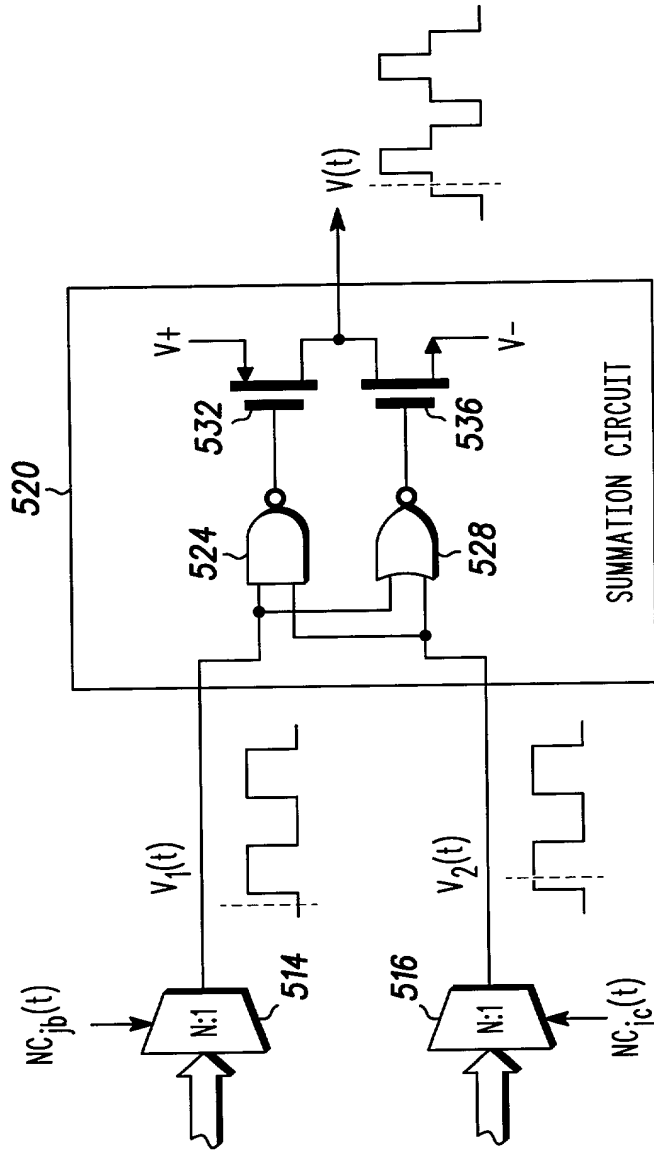


FIG. 10

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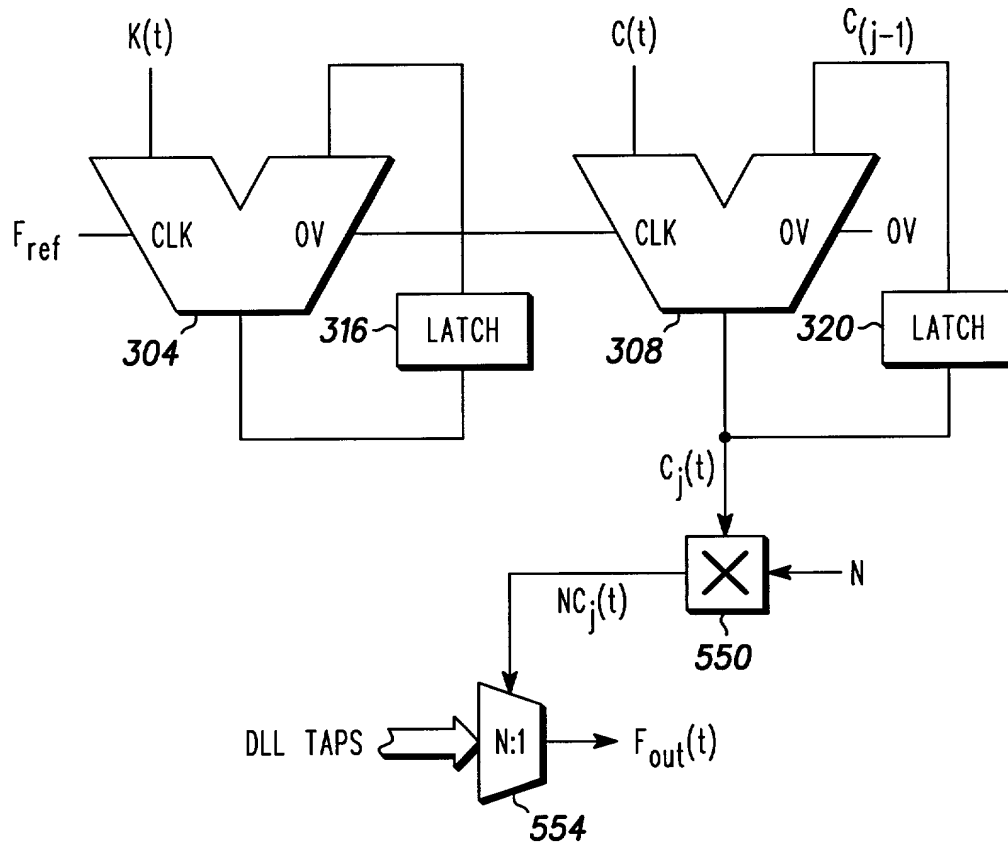


FIG. 11

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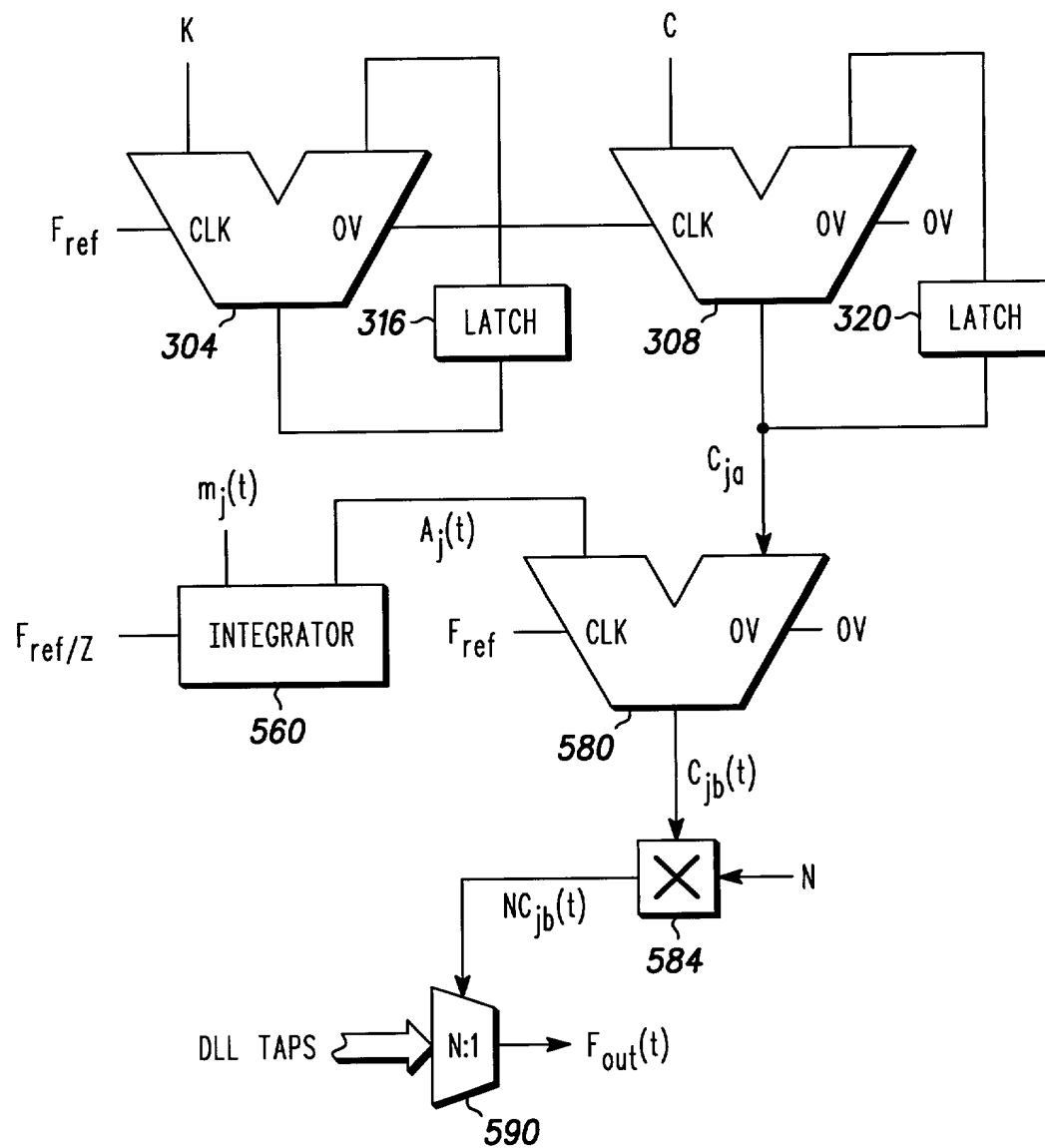


FIG. 12

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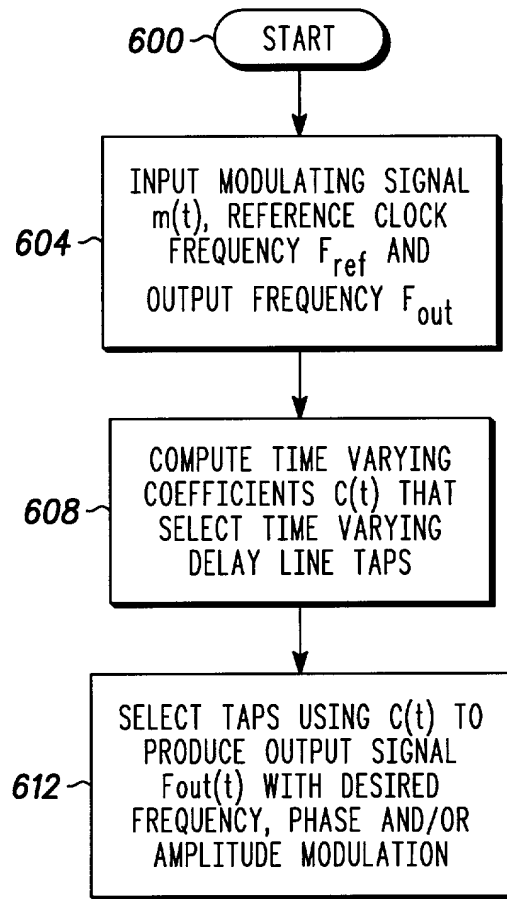


FIG. 13